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EXAMINER

BAYARD, EMMANUEL

ART UNIT PAPER NUMBER

2638

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/805,843

Applicant(s)

AUNG ET AL.

Examiner

Emmanuel Bayard

Art Unit

2638

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40,42-71 and 73-127 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-40,42-71 and 73-127 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

This is in response to amendment filed on 7/28/05 in which claims 1-40 and 42-71 and 73-127 are pending. The applicant's arguments have been fully considered but they are moot based on the new ground of rejection. Therefore this case is made final. (Also see examiner response to arguments below).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Azaren et al U.S. patent No 5,357,464.

As per claims 1 and 26, Azaren et al discloses an apparatus for receiving and processing a CDR signal comprising: an ICON circuitry is the same as the claimed (PLD circuitry) (see figs.1-2 elements 12, 34); first input configured to receive the CDR (see figs. 1-2 elements 16, 46 and col.4, lines 4-6, 48-54) signal; second input circuitry configured to receive an external reference clock signal (see figs.2-3 element SCLK and col.4, lines 3-6, 64-67); and Clock/data recovery circuitry is the same as the claimed (processing circuitry) (see fig.2 element 44. Note that recovery circuitry use the clock signal to recover the data signal) at least partly controlled by the PLD circuitry and configured to use the reference clock signal to recover data information from the CDR signal (see col.4, lines 45-67).

As per claims 2 and 27, Azaren et al does teach Wherein the PLD circuitry, the first and second input circuitries, and the processing circuitry are all integrated in a single integrated circuit device (See figs. 1-2 and col.1, lines 64-65)

As per claims 3 and 28, Azaren et al teaches wherein the first input circuitry comprises: phase locked loop circuitry (see fig.1 element 20)

As per claims 4 and 29, Azaren et al inherently teaches wherein the phase locked loop circuitry is programmable With respect to an operating parameter.

As per claims 5 and 30, Azaren et al inherently teaches wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

As per claim 6, Azaren et al inherently teaches wherein the second input circuitry comprises: phase locked loop circuitry

As per claim 7, Azaren et al inherently teaches wherein the phase locked loop circuitry is programmable with respect an Operating parameter.

As per claim 8, Azaren et al inherently teaches wherein the phase locked loop circuitry is configured to power down in response to a programmable power down signal.

As per claim 9, Azaren et al does teach wherein the first input circuitry comprises: further phase locked loop circuitry configured to receive an output signal of the phase locked loop circuitry and to produce a recovered clock signal that synchronized With the CDR signal (see fig.1 element 20 and col.5, lines 26-28).

As per claim 10, Azaren et al does teach wherein the further phase locked loop circuitry is further configured to adjust the phase of the output signal of the phase locked loop circuitry to produce the recovered clock signal (see fig.1).

As per claim 11, Azaren et al does teach wherein the processing circuitry comprises: deserializer circuitry configured to convert the data information from serial parallel form (see fig.9 element 102 and col.9, lines 53-58).

As per claim 12, Azaren et al inherently teaches wherein the deserializer circuitry is programmable with respect to an operating parameter.

As per claim 13, Azaren et al inherently teaches wherein the deserializer circuitry is further configured to reset in response to a reset signal selectively produced by the PLD circuitry.

As per claim 14, Azaren et al does teach wherein the processing circuitry comprises: buffer circuitry (see col.4, line 10 and col.8, line 13) configured to buffer the data information between a clock regime associated with reference clock signal and a different clock regime.

As per claim 15, Azaren et al inherently teaches wherein the buffer circuitry is further configured to signal selectively to reset in response a reset produced by the PLD circuitry.

As per claim 16, Azaren et al inherently teaches wherein at least one of the first input, second input and processing circuitries is configured to apply to the PLD circuitry a condition-monitoring signal indicative of an operating condition of that at least one circuitry.

As per claim 17, Azaren et al inherently teaches wherein at least one of the first input, second input, and processing circuitries includes a component that reset by a reset signal selectively produced by the PLD circuitry.

As per claim 18, Azaren et al inherently teaches wherein the first input circuitry further configured for alternate use receive a non-CDR data signal; the second input circuitry is further configured for alternate use to receive a non-CDR clock signal that is synchronized with the non-CDR data signal; and the processing circuitry further configured for alternate use derive the data information from the non-CDR data signal using the non-CDR clock signal.

As per claim 19, Azaren et al inherently teaches wherein the non-CDR data signal is an LVDS signal.

As per claim 20, Azaren et al inherently teaches further comprising: output circuitry configured to receive further data information from the PLD circuitry and to use the reference clock signal to encode the further data information as a further CDR signal for output by the apparatus. Not that the RX of Lee teaches a decoding process therefore it is inherent that an encoder process is included in the TX to further encode data information (see col.2, lines 5-14).

As per claim 21, Azaren et al teaches further comprising: loop-back circuitry configured selectively uses the further CDR signal as the CDR signal (see col.4, lines 14-15).

As per claim 22, Azaren et al teaches wherein the loop-back circuitry is configured so that it can be controlled by a signal from the PLD circuitry (see fig.1).

As per claim 23, Azaren et al inherently teaches further comprising: loop-back circuitry configured to selectively route the CDR signal for output by the apparatus in lieu of the further CDR signal.

As per claim 24, Azaren et al teaches wherein the loop-back circuitry is configured so that it can be controlled by a signal from the PLD circuitry (see fig.1).

As per claim 25, Azaren et al teaches wherein the loop-back circuitry is further configured for selective control by the PLD circuitry (see fig.1)

As per claim 31, Azaren et al inherently teaches wherein the output circuitry comprises: buffer circuitry (se) configured to buffer the data information between a clock regime associated with the PLD circuitry and a different clock regime associated With the reference clock signal.

As per claim 32, Azaren et al teaches wherein the output circuitry comprises: serializer circuitry configured to convert the data information from parallel to serial form (see fig.4 element 64).

As per claim 33, Azaren et al inherently teaches wherein the serializer circuitry is programmable with respect to an operating parameter.

As per claim 34, Azaren et al inherently teaches wherein at least one of the input and output circuitries is configured to apply to the PLD circuitry condition-monitoring signal indicative of an operating condition of that at least one circuitry.

As per claim 35, Azaren et al inherently teaches wherein at least one of the input and output circuitries includes a component that is reset by a reset signal selectively produced by the PLD circuitry.

As per claim 36, Azaren et al inherently teaches wherein the PLD circuitry is further configured to produce a non-CDR clock signal synchronized with the data information, and wherein the output circuitry is further configured for alternative use outputting the data information non-CDR form in parallel with the non-CDR clock signal.

As per claim 37, Azaren et al inherently teaches wherein output circuitry is further configured to selectively frequency-scale the non-CDR clock signal by a predetermined scale factor prior to outputting the non-CDR clock signal frequency-scaled form.

As per claim 38, Azaren et al inherently teaches wherein output circuitry is programmable with respect to the scale factor.

As per claim 39, Azaren et al inherently teaches wherein the non-CDR form of the data information is an LVDS signal.

As per claim 122, Lee et al discloses an apparatus for receiving and processing a plurality of CDR signals, each of which includes data information and clock information comprising: first circuitry (see figs 2-3. element 110a) producing a plurality of candidate recovered clock signals (see fig.4 recovered clock) from a reference clock signal (see element 204), the candidate recovered clock signals having phases that are shifted relative to one another; and a plurality of second circuitries (see fig.3 elements 302), each receiving a respective one of the CDR signals and using the candidate reference clock signals to recover the clock information from the CDR signal received by that second circuitry.

As per claim 123, Lee et al inherently teaches wherein the clock information of all of the CDR signals has a predetermined common frequency.

As per claim 124, Lee et al inherently teaches wherein the reference clock signal has frequency having a predetermined relationship to the predetermined common frequency.

As per claim 125, Lee et al inherently teaches wherein the first circuitry comprises phase locked loop circuitry.

As per claim 126, Lee et al inherently teaches wherein each of the second circuitries comprises: selection circuitry that selects at least one of the candidate recovered clock signals that is close in phase to the clock information in the CDR signal received by that second circuitry.

As per claim 127, Lee et al inherently teaches wherein each of the second circuitries comprises: selection circuitry that selects one of the candidate recovered clock signals that is closest in phase to the clock information in the CDR signal received by that second circuitry.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 102-121 are rejected under 35 U.S.C. 102(b) as being anticipated
Ariyavisitakul et al U.S. Patent No 5,084,891.

As per claim 102, Ariyavisitakul et al discloses a programmable serializer circuitry comprising: control circuitry that receives a programmable number (see figs. 9-10 element 930 and col.28, lines 61-65); input circuitry (see fig.10 element 1020) that receives a programmable number of input signals in parallel (see fig.10 element 8 and col.30, lines 26-30); and output circuitry (see fig.10 element 1020) that produces an output signal that is serially (see fig.10 element 1037 and col.30, lines 46-48) indicative of the input signals one after another.

As per claim 103, Ariyavisitakul et al does teach wherein the output signal is synchronized with a first clock signal having a first clock rate, and wherein the circuitry further comprises: clock rate divider circuitry that divides the clock rate by a programmable factor to produce a second clock signal for timing passage of information indicative of the input signals in parallel from the input circuitry to the output circuitry (see col.21, line 45-col.22, line 10 and col.30, lines 55-65)

As per claim 104, Ariyavisitakul et al inherently teaches wherein the factor is programmable to equal the programmable number.

As per claim 105, Ariyavisitakul et al teaches wherein the input circuitry comprises a predetermined plural quantity of register stages (see fig.10 elements 1025, 1030), and wherein the number is programmable to any integer value up to and including the plural quantity.

As per claim 106, Ariyavisitakul et al teaches wherein the register stages store the input signals in parallel (see col.21, lines 49-50).

As per claim 107, Ariyavisitakul et al teaches wherein the register stages further output in parallel to the output circuitry information indicative of the input signals (see col.30, lines 10-65).

As per claim 108, Ariyavisitakul et al teaches wherein the output circuitry comprises a predetermined plural quantity of register stages (see fig.10 elements 1025, 1030), and wherein the number is programmable to any integer value up to and including the plural quantity.

As per claim 109, Ariyavisitakul et al does teach wherein the register stages store in parallel information from the input circuitry indicative of the input signals (see col.30, lines 10-65).

As per claim 110, Ariyavisitakul et al does teach wherein the output circuitry further outputs information from the registers in a predetermined series one after another (see fig.10 and col.30).

As per claim 111, Ariyavisitakul does teach programmable serializer circuitry (see element 1020) and programmable logic circuitry (see fig.9 element 950 and col.28, lines 61-65) for supplying the input signals.

As per claim 112, Ariyavisitakul does teach Programmable deserializer circuitry comprising: control circuitry that receives a programmable number (see figs. 9-10 element 930 and col.28, lines 61-65); input circuitry (see fig.10 element 1040) that receives an input signal serially (see element 1037) indicative of plural bits of

information one after another and stores a programmable number of successive ones of Chose bits (see col.30, lines 48-50); and output circuitry (see element 1040) that produces a plurality of output signals in parallel (see element 1043), each of the output signals being indicative of a respective one of the bits stored by the input circuitry (see col.31, lines 25-27).

As per claim 113, Ariyavisitakul teaches wherein the input signal is synchronized with a first clock signal having a first clock rate, and wherein the circuitry further com clock rate divider circuitry that divides the clock rate by a programmable factor to produce a second clock signal for timing the passage of information indicative of the bits stored by the input circuitry in parallel from the input circuitry to the output circuitry (see col.30-col.31).

As per claim 114, Ariyavisitakul inherently teaches wherein the factor is programmable to equal the programmable number.

As per claim 115, Ariyavisitakul teaches wherein the input circuitry comprises a predetermined plural quantity of register stages (see elements 1025, 1030, 1040 and col.31, line 3), and wherein the number is programmable to any integer value up to and including the plural quantity.

As per claim 116, Ariyavisitakul inherently teaches wherein each of the register stages stores one of the bits.

As per claim 117, Ariyavisitakul inherently teaches wherein the register stages further output in parallel to the output circuitry information indicative of the bits stored in the register stages.

As per claim 118, Ariyavisitakul inherently teaches wherein the output circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

As per claim 119, Ariyavisitakul inherently teaches wherein the register stages store in parallel information from the input circuitry indicative of the bits stored by the input circuitry.

As per claim 120, Ariyavisitakul teaches wherein the output circuitry further outputs information from the registers in parallel (see col.31, lines 25-26).

As per claim 121, Ariyavisitakul does teach programmable deserializer circuitry (see fig.10 element 1040) and programmable logic circuitry (see fig.9 element 950) for receiving the output signals.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 40, 42-71, 73-101 are rejected under 35 U.S.C. 102(e) as being anticipated by Johansen U.S. Patent No 6,631,144 B1.

As per claims 40 and 71, Johansen teaches an apparatus for receiving an information signal which includes data information having clock information the data

information embedded in the data information comprising: first input circuitry configured receive the information signal (see fig.1 element 100 and col.15, lines 17-30); circuitry configured (see fig.1 element 300) to receive a programmable scale factor (see fig.1 element 50 and col.15, lines 41-60. Note that element 50 of Johansen generates number of scaling factors which are receive by element 300); second input circuitry configured receive a reference clock signal (see fig.1 element 70 and col.15, lines 44-60) having a reference frequency which is related to frequency of the clock information by a programmable scale factor; PLL is the same as the claimed (reference clock processing circuitry) (see fig.1 combined elements 330, 305, 310, 320 and col.15, lines 60-67 an col.16, lines 1-20) signal processing circuitry configured to use the information signal and the reference clock signal to produce recovered clock signal (see element 70) having phase and frequency which respectively correspond to a phase and frequency of the clock information; data reception is the same as the claimed (data recovery circuitry) (see fig.1 element 340 and col.16, lines 35-40. Note that element 340 of Johansen receives data information 220 and clock 335 to achieve properly synchronization process) configured to use the recovered clock signal and the information signal to produce a data output signal indicative of the data information in the information signal.

As per claims 42-43, Johansen inherently teaches: deserializer circuitry configured to convert the data output signal to a plurality of parallel data sub signals, each of which represents a respective portion of the data information indicated by the

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data output signal since the PLL can be arranged in parallel as taught by Johansen (see col.10, line 57).

As per claim 44, Johansen teaches further comprising: synchronizer circuitry (see col.16, lines 2, 35-36) configured to convert the data output signal to a further data output signal synchronized with a read control signal which can have phase and frequency substantially unrelated to the phase and frequency of the reference clock signal and the recovered clock signal.

As per claim 45, Johansen inherently teaches further comprising: selection circuitry configured to select as final data output signal either the data output signal or the further data output signal.

As per claim 46, Johansen teaches wherein the reference clock signal processing circuitry is further configured to use the scale factor producing the recovered clock signal (see col.16, lines 1-40).

As per claim 47, Johansen teaches wherein the reference clock signal processing circuitry is programmable with respect to the scale factor (see col.15, lines 46-60).

As per claim 48, Johansen inherently teaches wherein the information signal is applied to the first input circuitry as a pair of differential signals, and wherein the first input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal for further processing by the apparatus.

As per claim 49, Johansen inherently teaches wherein the reference clock signal is applied to the second input circuitry as a pair of differential signals: and Wherein the

second input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal for further processing the apparatus.

As per claims 50-51 Johansen teaches wherein the reference clock signal processing circuitry comprises: phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce a plurality of candidate further reference clock signals, each having the frequency of the clock information and having a phase which is different from the phases of the other candidate further reference clock signals (see col.15, line 63-67 and col.16, lines 1-67)).

As per claim 52, Johansen teaches wherein the further phase locked loop circuitry comprises: selection circuitry configured to select as the recovered clock signal the one of the candidate reference clock signals having the phase that works best with the phase of the clock information (see col.17, lines 39-50)).

As per claim 53, Johansen inherently teaches the data recovery circuitry comprises: register circuitry having a data input terminal to which the information signal is applied and clock input terminal to which the recovered clock signal applied, the register circuitry being configured to store and output samples of the signal applied to the data input terminal in synchronism with the signal applied to the clock input terminal.

As per claim 54, Johansen teaches the data recovery circuitry further comprises: buffer memory circuitry (see col.2, lines 45-46) configured to store multiple successive signal samples output by the register in synchronism with the recovered clock signal

and to output those samples the same order in response to another separate read clock signal.

As per claim 55, Johansen inherently teaches wherein the information signal represents successive words of J serial bits of data, and wherein the data recovery circuitry comprises: flip flop is the same as the claimed (shift register) (see fig.3) circuitry having a plurality of serially connected stages and configured to shift in successive samples of the information signal synchronism with the recovered clock signal; frequency divider circuitry configured to divide the recovered clock signal by J to produce a further reference clock signal and unload circuitry configured to unload all stages the shift register circuitry in parallel word form in synchronism with the further reference clock signal is inherently taught by Lee et al.

As per claim 56, Johansen inherently teaches divider circuitry is programmable wherein the frequency with respect to J.

As per claim 57, Johansen inherently teaches wherein the data recovery circuitry further comprises: buffer memory circuitry configured to store multiple successive parallel words from the unload circuitry in synchronism with the still further reference clock signal and to output those parallel words in a same order in response to another separate read clock signal.

As per claims 58, 61-62, 88 Johansen teaches further comprising: ASIC is the same as the claimed (PLD circuitry) (see fig.1 element 200) configured to use the data output signal.

As per claims 59, 89 Johansen teaches wherein all of the circuitries are disposed on a single integrated circuit (see col.12, lines 55-56).

As per claim 60, 90 Johansen inherently teaches further comprising: routing circuitry configured to selectively apply a signal indicative of the recovered clock signal to the PLD circuitry.

As per claim 63, Johansen inherently teaches first source of the information signal; a second source of the reference clock signal; first connection between the first source and the first input circuitry; and a second connection between the second source and the second input circuitry.

As per claim 64, Johansen inherently teaches wherein the first and second input circuitries are disposed on a common integrated circuit, which does not also include the first and second sources.

As per claim 65, Johansen inherently teaches wherein the information signal is a clock data recovery signal.

As per claim 66, Johansen inherently teaches further comprising: alternative reference clock signal processing circuitry configured to selectively alternatively produce a further reference clock signal based on the reference clock signal and without regard for the information signal (see fig.3).

As per claim 67, Johansen teaches; a buffer is the same as the claimed (memory) (see col.2, line 46)) coupled to said processing circuitry.

As per claim 68, Johansen inherently teaches a printed circuit board.

As per claim 69, Johansen inherently teaches further comprising: a memory mounted on the printed circuit board and coupled to the apparatus.

As per claim 70, Johansen inherently teaches further comprising: processing circuitry mounted on the printed circuit board and coupled to the apparatus.

As per claim 73, Johansen inherently teaches wherein the data source circuitry configured to produce the data signal as a plurality of parallel data sub signals (see col.10, line 58), each of which represents a respective portion of the data information, and wherein the data signal processing circuitry comprises: serializer circuitry configured to convert the plurality of parallel data sub signals to a single serial data signal is inherently taught by Johansen.

As per claim 74, Johansen inherently teaches wherein the serializer circuitry is programmable with respect to how many parallel data sub signals are converted.

As per claim 75, Johansen teaches wherein the data signal processing circuitry comprises: synchronizer circuitry (see col.16, lines 2-60) configured to receive the data signal in synchronism with a write control signal and to subsequently output the data signal in synchronism with the further reference clock signal, wherein the write control signal can have phase and frequency which are substantially unrelated to the phase and frequency of the reference clock signal and the further reference clock signal.

As per claim 76, Johansen inherently teaches wherein the data signal processing circuitry further comprises: selection circuitry configured to allow the data signal to selectively bypass the synchronizer circuitry.

As per claim 77, Johansen teaches wherein the reference clock signal processing circuitry is further configured to use the scale factor in producing the further reference clock signal (see fig.1).

As per claim 78, Johansen teaches wherein the reference clock signal processing circuitry is programmable with respect the scale factor (see col.15, lines 46-60).

As per claim 79, Johansen inherently teaches wherein the reference clock signal is applied to the input circuitry as a pair of differential signals, and wherein the input circuitry comprises differential driver circuitry configured to use the differential signals to produce a single output signal further processing by the apparatus.

As per claim 80, Johansen inherently teaches wherein the data signal processing circuitry comprises differential driver circuitry configured to transmit the information signal as a pair of differential signals.

As per claim 81, Johansen teaches wherein the reference clock signal processing circuitry comprises: phase locked loop circuitry configured to use the reference clock signal and the scale factor to produce the further reference clock signal (see figs.1-3 and col.16, lines 1-67)

As per claim 82, Johansen inherently teaches wherein the data signal processing circuitry comprises: register circuitry having a data input terminal to which the data signal is applied and clock input terminal to which the further reference clock signal applied, the register circuitry being configured to store samples of the signal

applied to the data input terminal and to output those samples in synchronism with the signal applied to the clock input terminal.

As per claim 83, Johansen inherently teaches wherein the data signal comprises a plurality of parallel data sub signals, each of which is indicative of a portion the data information, and wherein the data signal processing circuitry comprises: register circuitry having a plurality of data input terminals to Which the data sub signals are respectively applied and a clock input terminal to which the further reference clock signal is applied, the register circuitry being configured to store samples of the signals applied the data input terminals and to output those samples in series in synchronism with the signal applied to the clock input terminal.

As per claim 84, Johansen inherently teaches Wherein the data signal processing circuitry further comprises: buffer memory circuitry configured store multiple successive samples of each of the data sub signals in response to another separate write clock signal and to output those samples in the same order synchronism with the further reference clock signal.

As per claim 85, Johansen inherently teaches wherein the plurality of parallel data sub signals comprises J parallel data sub signals, and wherein the register circuitry comprises: shift register circuitry having a plurality of serially connected stages and configured to shift out contents of those stages in series in synchronism with the further reference clock signal; frequency divider circuitry configured divide the further reference clock signal by J to produce a still further reference clock signal; and load circuitry

configured to load, in parallel, all stages of the shift register circuitry with samples of the data sub signals in synchronism with the still further reference clock signal.

As per claim 86, Johansen inherently teaches wherein the frequency divider circuitry is programmable with respect to J.

As per claim 87, Johansen inherently teaches wherein the register circuitry further comprises: buffer memory circuitry configured to store multiple successive parallel words of samples of the data sub signals in response to another separate write clock signal and to output those parallel words a same order in response to the still further reference clock signal.

As per claim 91, Johansen inherently teaches further comprising: PLD circuitry configured to produce the write control signal.

As per claim 92, Johansen inherently teaches wherein PLD circuitry is further configured to include the data source circuitry.

As per claim 93, Johansen inherently teaches a first source of the reference clock signal; a second receiver of the information signal; a first connection between the first source and the input circuitry; and a second connection between the data signal processing circuitry and the second receiver.

As per claim 94, Johansen inherently teaches wherein the input circuitry and the data signal processing circuitry are disposed on a common integrated circuit, which does not also include the first source and the second receiver.

As per claim 95, Johansen inherently teaches wherein the information signals a clock data recovery signal.

As per claim 96, Johansen inherently teaches further comprising: alternative reference clock signal configured to produce an alternative source circuitry clock signal; signal selection circuitry configured to allow the alternative clock signal to be alternatively selectively used by the data processing circuitry as the further reference clock signal; output circuitry configured to output the alternative clock signal in parallel with the information signal.

As per claim 97, Johansen inherently teaches wherein the data signal processing circuitry comprises first differential driver circuitry configured to transmit the information signal as a first pair differential signals, and wherein the output circuitry comprises second differential driver circuitry configured to transmit the alternative clock signal as a second pair of differential signals.

As per claim 98, Johansen inherently teaches a memory coupled to said processing circuitry.

As per claim 99, Johansen inherently teaches a printed circuit board.

As per claim 100, Johansen inherently teaches further comprising: a memory mounted on the printed circuit board and coupled to the apparatus.

As per claim 101, Johansen inherently teaches further comprising: processing circuitry mounted on the printed circuit board and coupled to the apparatus.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shin et al U.S. Patent 5,974,464 teaches a system for high-speed serial video.

Riley U.S. Patent No 5,726,988 teaches a module with data verification.

New U.S. Patent No 5,999,025 teaches PLL architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM)
Alternate Friday off.

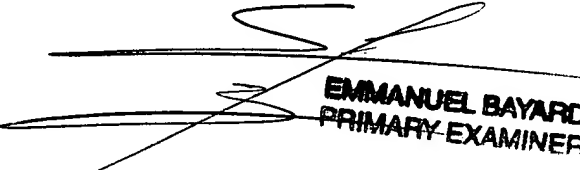
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2638

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

10/11/05



EMMANUEL BAYARD
PRIMARY EXAMINER